Guide to the HP48G/GX Hardware

Compiled by Philippe Teuwen

Version 0.90

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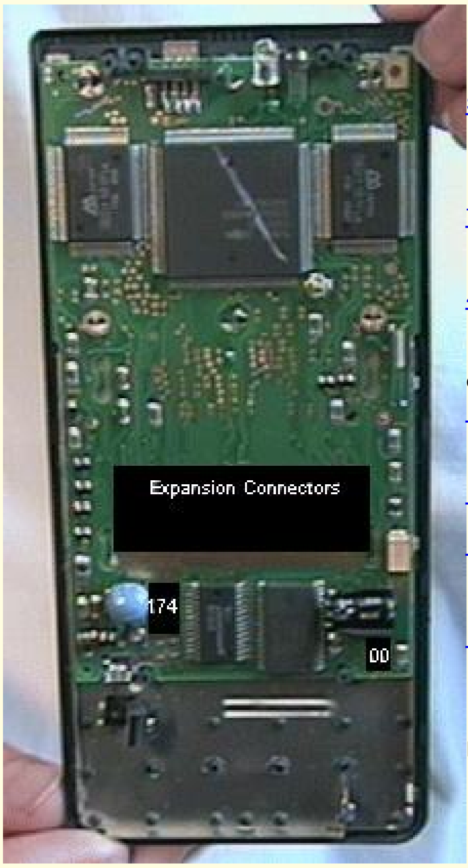
0. Table of contents

1. Introduction

These schematics result from personal observations.
So any warranties are provided about the content of this text.
Please notify me of any errors (about language too!) or omissions or to complete some points like official pins names and uses or bad known devices.
This text can be freely distributed but please don't modify it yourself.
Simply tell me what's wrong and I'll correct it for everybody.
All is shown from the back, batteries towards you unless you hear to the contrary.
Some parts exist only on GX calculators.

2. Global View

Note: This image is not clickeable in the PDF version



Serial connector/LED IR /Recv IR

The processor between 2 LCD drivers

4 jumpers disseminated on the PCB

crystal (32 kHz time X'tal)
RX IR Circuits on the right

RS 232 Circuits on the left

Expansion connectors

From left to right:
Power Supply/74HC174 /RAM/ROM /Capacitor 1mF/74HC00

Battery Case

3. Pin outs Description

A0-A16	Address lines
A17-A21	Extended lines for port 2 (A18 is inverted, actually: NA18)
AR17-AR18	Extended lines for ROM
BEN	Bank Switching Enable
buzz	Buzzer (the second line of the buzzer is grounded)
CDT1-CDT2	Card Detect Type for port 1-2 (H:RAM L:ROM X:No Card)
CE1	Card Enable 1 (In GX, is used to enable A17-A21 for port 2)
CE2	Card Enable 2 (In GX, is used as CE for port 1)
CE2.2	Card Enable port 2 (Not from CPU; CE2.2=BEN*N(AR18))
ChkBat	Probes the boost-switching power supply
D0-D7	Data lines
DrvBat	Drives the MOSFET of the boost-switching power supply
GND	Ground
LD(0)	Display: The first bit of display information

LD(1)	Display: The next bit LP: Display horiz sync (Fall. edge: a new line is about to be started)
NC	Not Connected
NCE0	Card RAM Enable
NCER	?Card ROM Enable
NOE	Original Output Enable (Not used in G/GX)
NOE2	Output Enable for all RAMs and ROM (Not from CPU; NOE2=N(NWE))
NWE	Write Enable for all RAMs
ON-key	ON-key is wired directly to CPU
RX	RS232 Reception
RXir	IR Reception
SPD	Processor Speed (H:4MHz L:2.4MHz)
sync1	?Display sync line (between both drivers)
sync2	?Display sync line (between both drivers)
sync3	?Display sync line (between both drivers and the CPU)
sync4	?Display sync line (between both drivers and the CPU)
sync5	?Display sync line (between both drivers and the CPU)
TX	RS232 Transmission
TXir	IR Transmission
V1-V299	Display data lines for the LCD
Vbat	Directly wired from battery + pin
Vbb1-Vbb2	Card battery check (L:warning low bat port 1-2)
Vco	=5V if HP is turned on else =0V
Vdd	=5V if HP is turned on else =4.5V(bat)
Vh	=10V if HP is turned on else =4.5V(bat)
XSCL	Display clock (Falling edge: 2 bits of display data may be read)
Xtal1	To X'tal 32kHz
Xtal2	To X'tal 32kHz
(GND)	Ground (pin out of the RS232 I/O)
(RX)	Reception (pin out of the RS232 I/O)
(SH)	Shield (pin out of the RS232 I/O)
(TX)	Transmission (pin out of the RS232 I/O)

4. 74HC174: Hex D-type flip-flop with clear (Only on GX)

Ext.	Pin	Int.	74HC174 upside down	Int.	Pin	Ext.

CE1	9	CLK		GND	8	GND
BEN	10	4Q		3Q	7	A17
A5	11	4D		3D	6	A0
A21	12	5Q		2Q	5	A18
A4	13	5D		2D	4	A1
A3	14	6D		1D	3	A2
A20	15	6Q		1Q	2	A19
Vco	16	Vdd		NCLR	1	Vdd 3V

Vdd 3V is just made by a voltage divider: `GND --- 100k --- Vdd 3V --- 47k --- Vco`

NCLR	CLK	D	Q
L	X	X	L
H	^	H	H
H	^	L	L
H	L	X	Q0

5. 74HC00: Quad 2-input NAND gate (Only on GX)

Ext.	Pin	Int.	74HC00	Int.	Pin	Ext.
Vco	1	1A		Vdd	14	Vco
AR18	2	1B		4B	13	Vco
4(HC00)	3	1Y		4A	12	NWE
3(HC00)	4	2A		4Y	11	NOE2
BEN	5	2B		3B	10	6(HC00)
10(HC00)	6	2Y		3A	9	Vco
GND	7	GND		3Y	8	CE2.2

Logic: Y=N(A*B)

Results: CE2.2=BEN*N(AR18) and NOE2=N(NWE)

6. RAM 32k(G) or 128k(GX) ROM 512k

Ext.	Pin 128/32	Int.	RAM 32/128 upside down	Int.	Pin 32/128	Ext.
D3	17/15	D3		GND	14/16	DIV ALIGN=right> GND

D4	18/16	D4		D2	13/15	D2
D5	19/17	D5		D1	12/14	D1
D6	20/18	D6		D0	11/13	D0
D7	21/19	D7		A0	10/12	A0
NCE0	22/20	NCE		A1	9/11	A1
A10	23/21	A10		A2	8/10	A2
GND	24/22	NOE		A3	7/9	A3
A11	25/23	A11		A4	6/8	A4
A9	26/24	A9		A5	5/7	A5
A8	27/25	A8		A6	4/6	A6
A13	28/26	A13		A7	3/5	A7
NWE	29/27	NWE		A12	2/4	A12
Vdd	30/28	CE/Vdd		A14	1/3	A14
			32 stops here			
A15	31/*	A15		A16	*/2	A16
Vdd	32/*	Vdd		NC	*/1	GND

Ext.	Pin	Int.	ROM 512k upside down	Int.	Pin	Ext.
D3	17				16	GND
D4	18				15	D2
D5	19				14	D1
D6	20				13	D0
D7	21				12	A0
NCER	22				11	A1
A10	23				10	A2
GND	24				9	A3
A11	25				8	A4
A9	26				7	A5
A8	27				6	A6
A13	28				5	A7
A14	29				4	A12
AR17	30				3	A15

AR18	31				2	A16
Vco	32				1	GND

7. Ports (Only on GX)

Two 40-pin card connectors for plug-in cards :
For ease of expanding the HP48's capabilities, dual 40-pin connectors are installed on the logic board.
These connectors will accept credit-card-size plug-in RAM or ROM cards.
Each connector has its own chip select line but all address and data lines are common to the internal ICs.
The 1LT8 tests the connectors to determine if a card is present and if it is write protected.
It does this by checking the card's write protect output. If the write protect signal is high, a card is plugged in and can be written to (RAM).
If the output is low, a card is present and is write protected (RAM or ROM).
If the line is floating, no card is present.
RAM cards have their own lithium keep-alive batteries.
When the HP48 goes into deep sleep, the power supply to the cards (Vco supply) is turned off.
When the supply drops to between 3.9 and 3.5V, the RAM switches to its internal battery.
The lithium voltage is sampled by the 1LT8, and when it drops to between 2.5 and 2.2V, a low-battery annunciator is turned on.

Pin	Port 1	Port 2
1	Vco	Vco
2	Vbb1	Vbb2
3-19	A0-A16	A0-A16
20	NWE	NWE
21	CE2	CE2.2
22	NOE2	NOE2
23-30	D0-D7	D0-D7
31	AR17	A17
32	AR18	A18
33	XSCL	A19
34	LP	A20
35	LD(0)	A21
36	LD(1)	BEN
37	CDT1	CDT2
38	NC	NC

39	NC	NC
40	GND	GND

In Seiko-Epson Cards: pin 38: Card Present, pin 39: Card Type

8. Drivers for LCD

Column drivers

Refs: SED1181Fla Japan

The 64-row-by-131-column STN LCD is driven by two commercial column drivers, each driving 64 columns, and the 1LT8 which drives 64 rows, 3 columns and 7 annunciator lines.
The column drivers receive their data, timing and control signals, and voltage levels from the 1LT8.
One of the problem with the commercial column drivers is that they require a negative voltage.
To overcome this, their + V line are connected to Vh (~10V) supply, their GND to Vdd (~5V) and their negative supply to GND.
This requires all data and control signals received from the 1LT8 to swing from 4.4V to 8.5V.
Display data is stored in system RAM, and the 1LT8 display controller interrupts the CPU for 22 to 23µs every 244µs (SX) to access it.
As display data is received, it is serially shifted to the column drivers.
When the column drivers have received 128 bits of data, they store it and output it to the display synchronously with a row driver output from the 1LT8.

	Left (reversed)	**Right**
1-28	V254-V281	V222-V249
29	sync2	NC
30	NC	NC
31	NC	NC
32	LD(0)	sync1
33	LD(1)	sync2
34	XSCL	XSCL
35	LP	LP
36	sync3	sync3
37	V87	V52
38	V86	V51
39	V85	V50
40	V83	V49
41-50	V82-V73	V47-V38

51	V71	V37
52	V70	V36
53-62	V69-V60	V34-V25
63	V58	V24
64-68	V57-V53	V22-V18
69	sync4	sync4
70	sync5	sync5
71	sync5	sync5
72	Vdd	Vdd
73	Vh	Vh
74	sync1	NC
75	NC	NC
76	NC	NC
77-80	V250-V253	V218-V221

9. Keyboard

```
Mylar domed keyboard with carbon graphite traces
Refs: MXS 00048-80038
! on the other side of the PCB, so X'tal is on the left
```

17 pads:

1	Vdd	7	A3	13	A1
2	ON-key	8	A11	14	A15
3	A5	9	A12	15	A16
4	A4	10	A2	16	A0
5	A10	11	A13	17	AR17
6	A9	12	A14		

Pressing a key makes a shortcut between 2 lines.
The 49-key keyboard is scanned by the Yorke chip via multiplexed RAM and ROM address lines.
Address lines A9 to AR17 scan the keyboard while A0 to A5 are inputs to the Yorke.
The keyboard is read asynchronously every millisecond when the CPU drives its output register lines, A9 to AR17, all high and reads its input register lines, A0 to A5.
When a key is pressed, contact is made between an input register line and an output register line, putting a high level on the input register line.
This high level generates an interrupt, causing software to scan the keyboard to determine which key is pressed.
The ON key is not scanned but is wired to Vdd.

This allows the system to be turned on while in deep sleep.
The ON key is the only key capable of generating an interrupt and waking the system up.
All key lines are isolated from the main system address lines by built-in 4-kohms carbon graphite resistors.

Correspondence Table:

A	B	C	D	E	F
O A10 I A4	O AR17 I A4	O AR17 I A3	O AR17 I A2	O AR17 I A1	O AR17 I A0
MTH	PRG	CST	VAR	up	NXT
O A11 I A4	O A16 I A4	O A16 I A3	O A16 I A2	O A16 I A1	O A16 I A0
'	STO	EVAL	left	down	right
O A9 I A4	O A15 I A4	O A15 I A3	O A15 I A2	O A15 I A1	O A15 I A0
SIN	COS	TAN	sqrt	Y^X	1/X
O A12 I A4	O A14 I A4	O A14 I A3	O A14 I A2	O A14 I A1	O A14 I A0
ENTER		+/-	EEX	DEL	back
O A13 I A4		O A13 I A3	O A13 I A2	O A13 I A1	O A13 I A0
alpha		7	8	9	/
O A12 I A4		O A12 I A3	O A12 I A2	O A12 I A1	O A12 I A0
shift left		4	5	6	*
O A11 I A5		O A11 I A3	O A11 I A2	O A11 I A1	O A11 I A0
shift right		1	2	3	-
O A10 I A5		O A10 I A3	O A10 I A2	O A10 I A1	O A10 I A0
ON		0	.	SPC	+
O Vdd I ON-key		O A9 I A3	O A9 I A2	O A9 I A1	O A9 I A0

ML Correspondences:

	#001	A9
	#002	A10
	#004	A11
	#008	A12

OUT:	#010	A13
	#020	A14
	#040	A15
	#080	A16
	#100	AR17
IN:	#0001	A0
	#0002	A1
	#0004	A2
	#0008	A3
	#0010	A4
	#0020	A5
	#8000	ON-key

10. LCD Display

```
Refs: LD-F8845A-23 363D Epson Japan
! on the other side of the PCB, so X'tal is on the left
```

202 pads:

up:	1-105	V1-V105
down:	201	V201
	202	NC
	203-297	V203-V297
	298	NC
	299	V299

11. Yorke Chip

```
Refs: 00048-80063 D3004GD NEC Japan
```

The SX one is also know as the 1LT8

Contains the CPU, an LCD driver controller, a memory controller, and a UART for RS-232 and IR I/O control.

1	NC	90	NWE	137	LD(0)
2	NC	91	RESET (if low)	138	LD(1)
3	TXir	92-99	D0-D7	139	V88

4-18	V217-V203	100	AR17	140	V282
19	V201	101-117	A16-A0	141	V89
20-35	V16-V1	118	Xtal2	142	NC
36	NC	119	Xtal1	143	sync5
37	SPD	120	NC	144	sync4
38	NC	121	NOE	145	Vbat
39	V84	122	TXir	146	Vbb2
40	V72	123	GND	147	Vbb1
41-56	V90-V105	124	ChkBat	148	Xtal1
57	V299	125	Vdd	149	Xtal2
58-72	V297-V283	126	Vco	150	CDT1
73-80	NC	127	NCER	151	CDT2
81	RX	128	DrvBat	152	V17
82	TX	129	-1.5k-buzz	153	V23
83	XSCL	130	Vh	154	V35
84	ChkBat	131	TX	155	V48
85	AR18	132	GND	156	V59
86	ON-Key	133	RX	157	V72
87	CE2	134	XSCL	158	V84
88	CE1	135	LP	159	GND
89	NCE0	136	sync3	160	RXir

12. Printed Circuit Board

Refs: 00048-80050

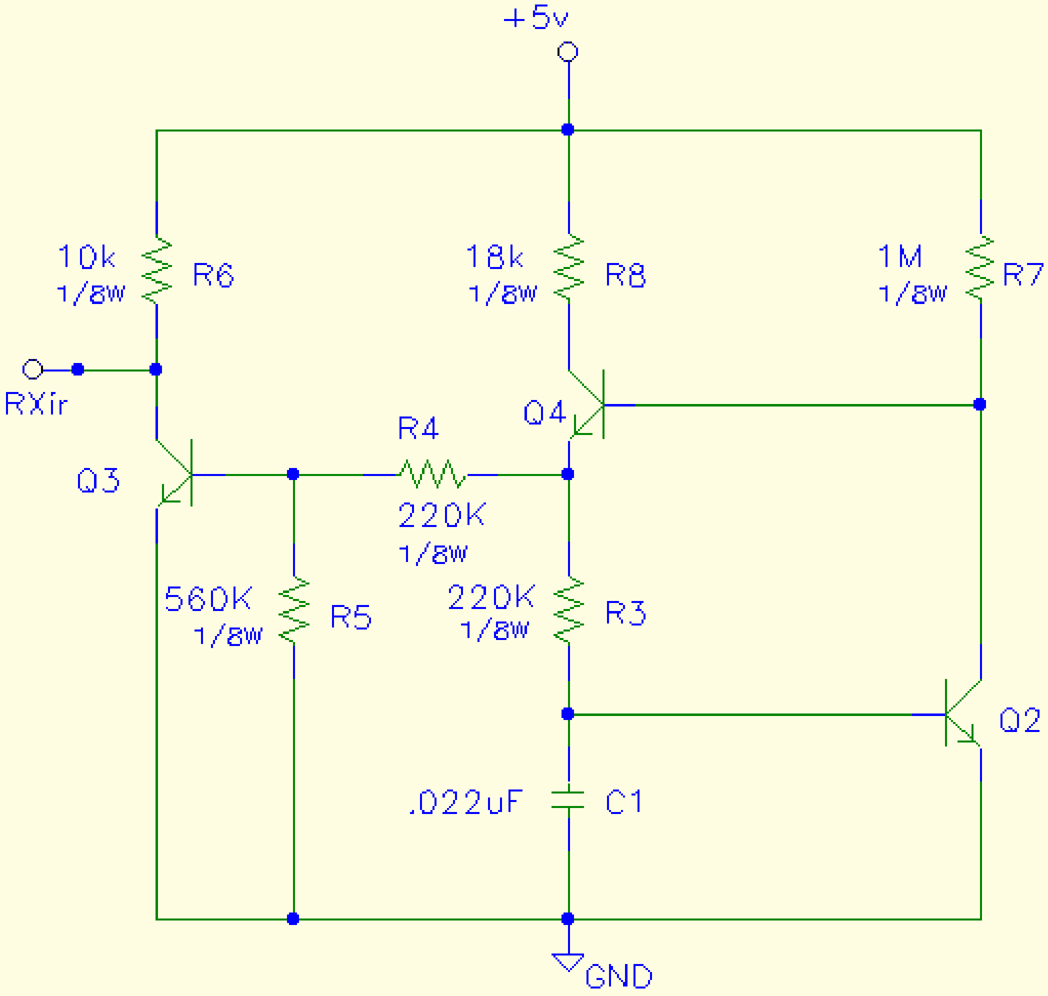
The printed circuit board measures 5.1 inches by 2.75 inches (13 * 7 cm) for the SX
and 5.25 inches by 3 inches (13.3 * 7.6 cm) for the GX
For production testing, main logic boards traces have dual test points.
These test points are probed by a special test block that is connected to an HP 3065 test system.
The HP 3065 tests all discrete components and ICs before the unit goes to final assembly.(SX)

Some tracks are interlaced to allow to solder a bridge on it.

These jumpers exist to allow to construct easily a SX with this PCB.

```
Left one :   CE1<->CE2.2
Right one :  NOE<->NOE2
Middle one : SPD<->Vdd CPU at 4MHz (soldered originally)
Upper one :  SPD<->GND CPU at 2.4MHz
! Never solder these two last ones at the same time.
```

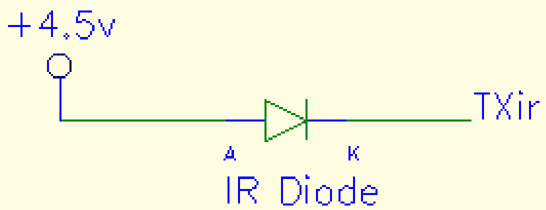
13. IR Reception



Q1,Q2,Q3: 2N3904

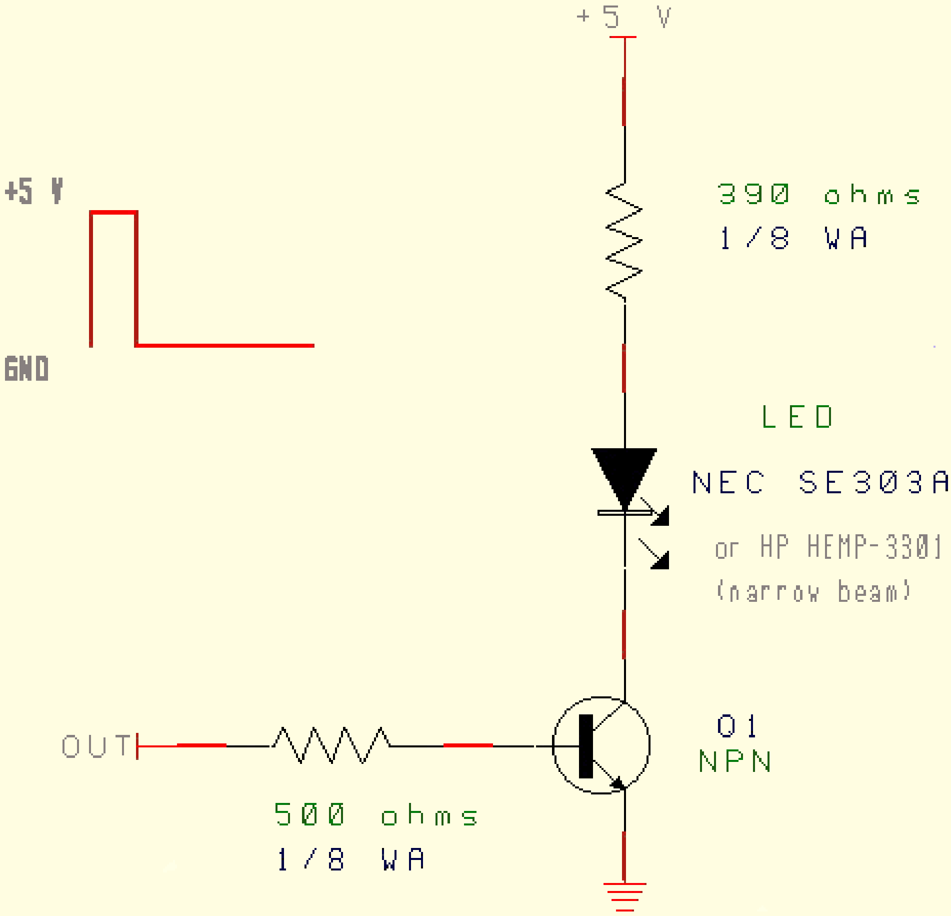
Q4: Receiver
Refs: EG&G VATEC VTT 9112

14.1 IR Transmission for the G/GX



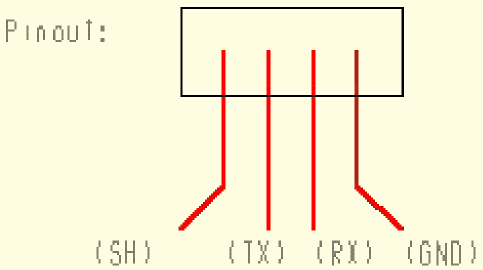
14.2 IR Transmission for the S/SX

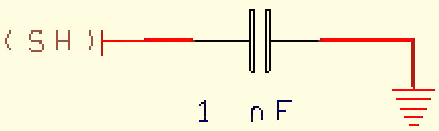
Rem: schema picked up from HP I/O Technical Interfacing Guide

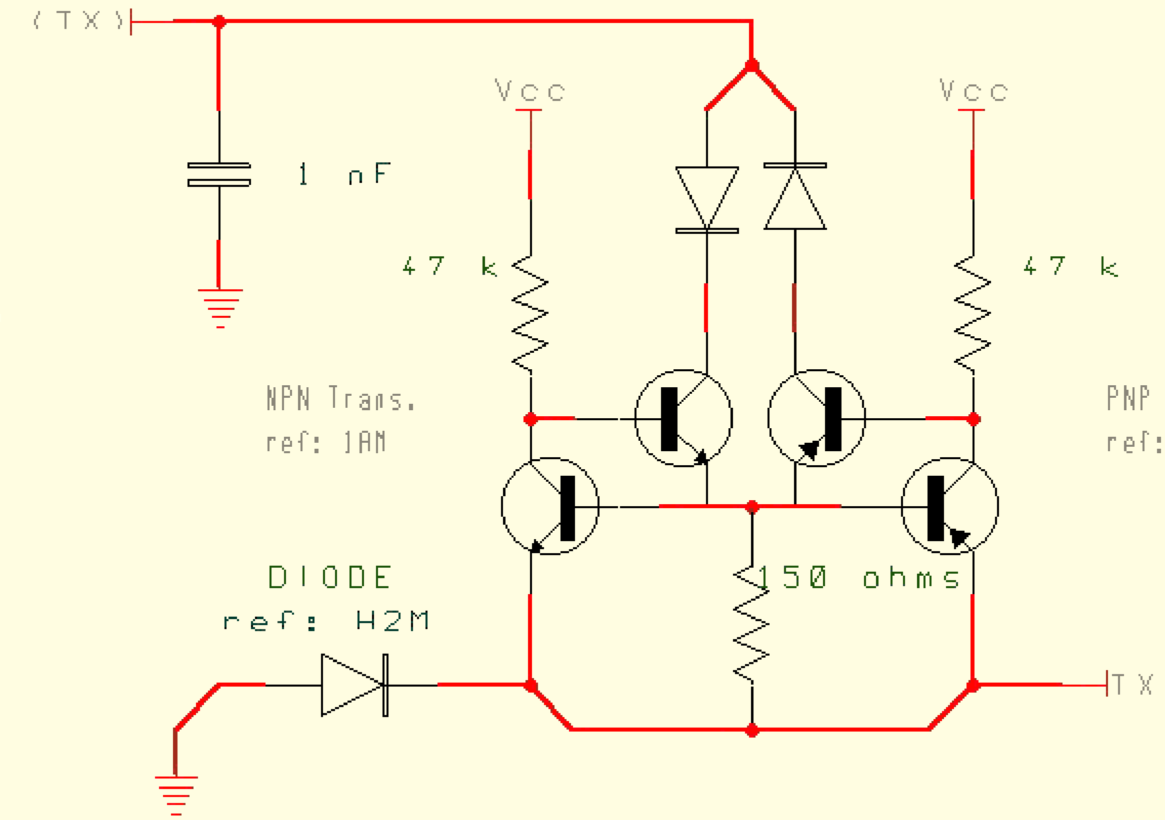


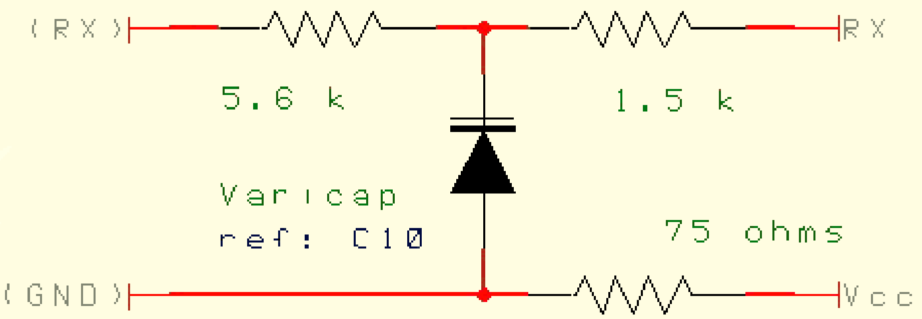
15. RS232 Description

Four-pin RS-232 connector:









16. Power Supply

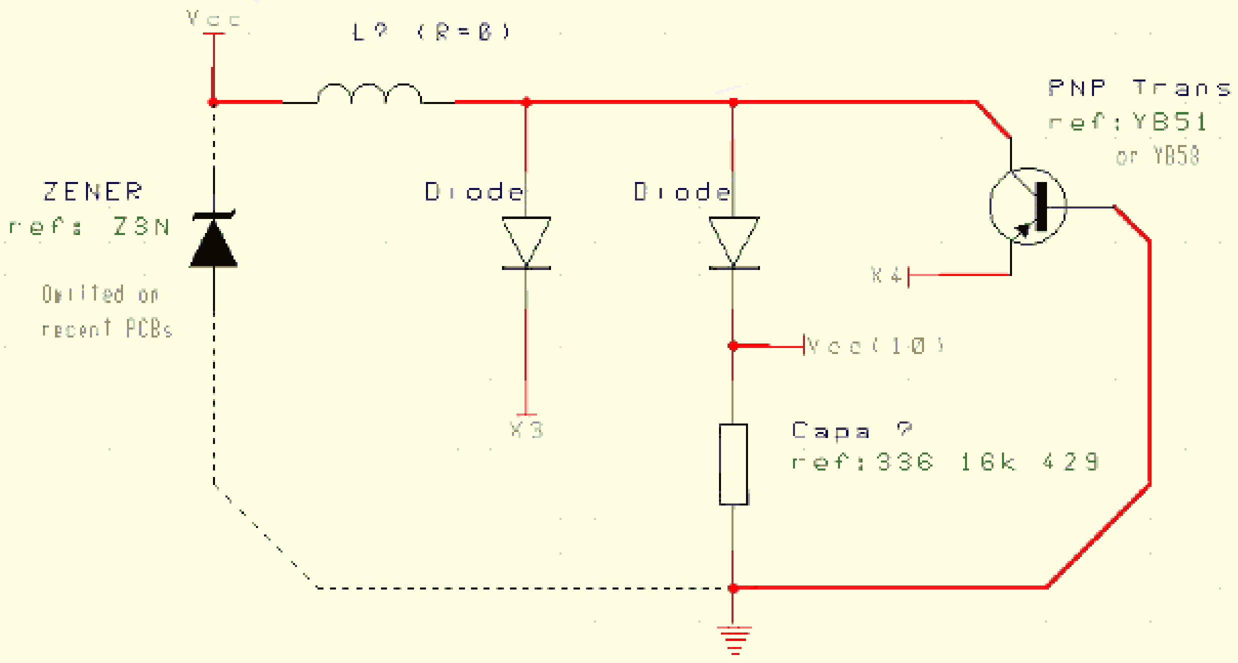
The system is powered by three AAA batteries and has three power supplies, which are controlled by the Yorke chip.
The Vh(~10V) supply is used for the LCD display and RS-232 voltage swings.
The Vdd(~5V) is the main logic supply.
The Vco(~5V) supply is derived from the Vdd supply and is used to power the ROM and plug-in cards mainly.
The power supply requires only two discrete diodes, an inductor, an n-channel power MOSFET, and three filter capacitors.
This is a boost-switching power supply in which the Yorke chip controls the current in an inductor, which is connected to the batteries, via the MOSFET.
When one of the supplies (Vh or Vdd) is low, the Yorke pulses the MOSFET at a 122.84kHz (for SX) rate, increasing the inductor current.
The current from the inductor is then dumped through one of the diodes, charging its filter capacitor.
If both supplies are low the Yorke switches the charge between them at a 30.72-kHz rate.

To conserve battery life, the power supplies (and the product) have three modes of operation:

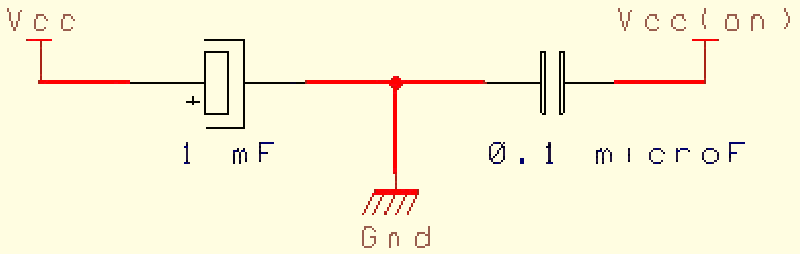
- Running.
  The 1LT8, column drivers, RAM and ROM, power supplies, and plug-in ports are all powered.
- Light sleep.
  In this mode the 1LT8 turns off, this mode is entered whenever the CPU is inactive and a key is not being pressed.
  The 1LT8's display controller accesses memory every 244µs to update the display.
  When the update is complete, the address lines switch and check to see if a key is pressed.
  Pressing any key will turn the CPU on.
- Deep sleep.
  All supplies are turned off.
  The Vdd supply floats to the battery voltage (Vbat) which supplies power to the ON key, 1LT8, and RAM.
  This mode is entered when the CPU has been inactive for ten minutes or the unit has been turned off.
  To wake the system, the ON key must be pressed.
- There is also a fourth mode: Really deep sleep, brought by pressing ON and SPC keys, even the clock stops working.
  To wake the system, the ON key must be pressed.

The1LT8 chip also monitors the battery voltage.
When the voltage falls to between 3.4 and 3.0 volts, the low-battery annunciator is turned on.
If the batteries are not changed and the battery voltage falls below 1.5 volts, the system turns off.
A 1000-µF capacitor maintains the Vdd supply for several minutes while the batteries are being changed.

Warning!
The schematic is partially wrong! please wait for the right one.
x4 and the base must be switched
x3 is ChkBat and x4 is DrvBat and the voltage lines have their name changed
the zener is not omitted on recent PCBs but simply physically moved in another place! (5.6V)
the self is 1.2mH
the transistor is a MOSFET



17. Backup Power Supply



18.1

```
When a current larger than ~120mA flows through the CPU, all the indicators will be
set independently of the HP state.
```

19. Contacting the author

Note: this section has been updated in 2016.


```
Philippe TEUWEN
Email: phil@teuwen.org
Twitter: @doegox
Website: http://www.yobi.be
```


20. Contributors

Note: all these references are dead in 2016.

Elbert S. Liu : he made good looking schematics GIF for the IR part
Matthew Mastracci : he helped me for some language mistakes
Christian Daniel : He corrected a missed part in the RS232 circuitry and gave me wonderful docs from HP about the SX.